



#4
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit : 2815
Applicants : Kazuo AOYAMA, et al.
Serial No. : 09/754,632
Filed : January 4, 2001
For : FUNCTION RECONFIGURABLE SEMICONDUCTOR
DEVICE AND INTEGRATED CIRCUIT CONFIGURING
THE SEMICONDUCTOR DEVICE

Assistant Commissioner for
Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.56

S I R :

Applicants wish to bring to the attention of the
Examiner the following publications:

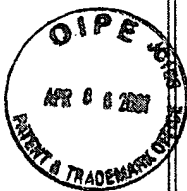
1. Hiroshi Sawada, Kazuo Aoyama, Akira Nagoya and
Kazuo Nakajima, "Consideration for a Reconfigurable Logic
Device using Neuron MOS Transistor", TECHNICAL REPORT OF
IEICE. CPSY99-89, pp. 41-48, November 27, 1999.

2. Kazuo Aoyama, Hiroshi Sawada, Akira Nagoya and
Kazuo Nakajima, "A Design Method for a Circuit with Neuron MOS
Transistors Realizing any Symmetric Function", TECHNICAL
REPORT OF IEICE. CPSY99-90, pp. 49-56, November 27, 1999.

3. Kazuo Aoyama, Hiroshi Sawada, and Akira Nagoya
"A Method for Designing a Circuit with Neuron MOS Transistors
Realizing any Logic Function", The 13th Workshop on Circuits
and Systems in Karuizawa, pp. 113-118, April 24-25, 2000.

4. Kazuo Aoyama, Hiroshi Sawada, and Akira Nagoya
"A Design of a Circuit with Neuron MOS Transistors Realizing
any Symmetric Function", PROCEEDINGS OF THE 2000 IEICE GENERAL
CONFERENCE, p. 85, March 31, 2000.

5. Japanese laid-open patent application No. 7-
161942.



6. Japanese laid-open patent application No. 6-77427.

7. Kazuo Aoyama, Hiroshi Sawada, Akira Nagoya, and Kazuo Nakajima, "A Threshold Logic-Based Reconfigurable Logic Element with a New Programming Technology", 10th International Conference, FPL 2000, pp. 665-674, August 30, 2000.

8. Tadashi Shibata, and Tadahiro Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 39, No. 6, pp. 1444-1455, June, 1992.

9. Tadashi Shibata, Koji Kotani, Tadahiro Ohmi, "Real-Time Reconfigurable Logic Circuits Using Neuron MOS Transistors," International Solid-State Circuits Conference, 1993.

10. S.D. Brown, et al. "Field-Programmable Gate Arrays," Kluwer Academic Publishers.

These publications are listed on the attached form PTO-1449 and copies are enclosed for the convenience of the Examiner, along with English translations of the foreign publications.

It is requested that these publications be considered and made of record herein.

The Office is hereby authorized to charge Deposit Account No. 11-0600 for any fees required by this paper, a copy of which is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on

Date

Apr 3, 2001 Atty's Reg. # 18,918

Atty's Signature

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Respectfully submitted,

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